REMARKS

Claims 1-44 are pending. Claims 1-7, 11, 12, 14-22, 26, and 37-40 including independent claims 1 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Dick (6,600,788). Dependent claims 8-10, and 23-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung ("An integrated CAD System for Algorithm-Specific IC Design", IEEE Transactions on Computer Aided Design, Vol. 10, No. 4, April 1991). Claims 13, 27-29, and 41-44 including independent claim 41 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Shung and further in view of Saramaki ("Design of Computationally Efficient Interpolated FIR Filters, IEEE Transactions on Circuits and Systems, Vol. 35, No. 1, January 1998).

The Examiner notes that an associated provisional patent application serial number has not been listed on the Oath/Declaration. An application data sheet is being filed to address this concern.

The Examiner objected to claims 2-6 and 17-20 for formality reasons. Claims 2-6 and 17-20 have been amended to address formality concerns. The objections are believed overcome. The Examiner objected to claim 1 for antecedent basis reasons. Claim 1 has been amended to overcome this objection.

In a previous Office Action response, the Applicants argued that none of the references cited by the Examiner or the previous Examiner assigned to the case teach or suggest a "filter resource estimator." Furthermore, none of the references cited teach or suggest a "resource estimator is coupled to the filter spectral response simulator." The Examiner does not argue that a "resource estimator" is taught or suggested and does not cite any new references but instead maintains the 102(e) and 103(a) rejections because the Examiner argues that the filter resource estimator is vaguely defined in the present application.

More specifically, the Examiner rejects claims 1-44 under 35 U.S.C. 112(1) as failing to comply with the written description requirement and enablement requirement. The Examiner argues that the specification merely mentions a filter resource estimator without definition.

The Applicants respectfully submit that "filter resource estimator" is described throughout the present application and the description is sufficient to enable one of skill in the art to make of use the invention.

Figure 3 details implementing a FIR filter by estimating filter resources. According to various embodiments, Figure 3 and associated description (page 16, line 23 - page 17, line 13) note specifically that "Once the appropriate architecture is selected for implementing the selected FIR filter, an estimate is made at 516 of the resources to be utilized in implementing the FIR filter in the selected architecture. By resources, it is meant those resources, such as programming, memory, logic, that must be used to implement the particular FIR filter. Once the resources to be used are estimated, a determination is made whether or not the amount of resources estimated to be used is acceptable at 518. If it is determined that the estimated amount of resources is not acceptable, then a determination is made at 520 whether or not the filter hardware (i.e., the basic FIR filter design itself) is to be updated. If it is determined that the filter hardware is to be updated, then control is passed back to 510, otherwise control is passed back to 514, and repeat steps starting at 516. Returning to 518, if it is determined that the estimated resources to be used in implementing the FIR filter is acceptable, then the particular FIR filter design is compiled at 522. Once compiled, the FIR compiler provides a simulation file at 524 and a hardware file at 526."

Figure 6 and associated description further describe a filter resource estimator in detail specifying examples for calculating resources (e.g. the number of logic cells or EABs) used to implement a filter. According to various embodiments, Figure 6 and associated description (page 20, line 16 - page 21, line 14) note "Once the performance of a particular FIR filter designed is deemed acceptable an estimate of the resources required to implement the particular designed as detailed by a flowchart of a process 800 as shown in Fig. 6. ... After the symmetry (or lack thereof) of the FIR filter is determined, a determination is made at 816 of the filter type. If the filter is a parallel filter, then the size of the parallel tap delay line is determined at 818 and the coefficients are divided into groups at 820 based upon the reasons stated above with regards to process 700. At 822, the size of the ROM LUT for partial products is determined and at 824, the size of the adder tree for the partial products is determined. At 826, a determination is made whether or not there are more groups of coefficients. If there are more coefficients, then control is passed to 822, otherwise, the size of the additions of the previous adder trees of partial products for all groups is determined at 828. At 830, the number of logic cells required to

implement the FIR filter is calculated. Returning to 816, if the filter is a serial filter, then the size of the serial tap delay line is determined at 832 based upon either EABs or logic cells and the coefficients are divided into groups at 834. At 836, the size of the adder tree for all groups is determined and at 838, the size of the scaling accumulator for n clock cycles is determined and at 840. At 842, the number of logic cells or EABs required to implement the FIR filter is then calculated."

Figure 14 shows estimated filter resources. According to various embodiments, Figure 14 and associated description (page 24, lines 10-15) note that an estimation of filter resources is shown "Display the result of this calculation in a RESOURCE USAGE display 1602 showing, for this example, the estimated size in Embedded Array Blocks (EABs) and/or logic cells and the number of clock cycles required to perform the FIR computation. In a particular embodiment, the latency (i.e., the number of clock cycles before the output is available) is output to a report file."

The detailed description noted above and in other portions of the specification not noted is provided in conjunction with a higher level description noted on (page 10, lines 19 – 25). "In a preferred embodiment, the cost analysis is performed substantially in parallel with the performance analysis. By "cost" it is meant the total number of resources (programming, memory, logic, etc.) required to implement the particular filter design whereas a performance analysis can involve determining speed, power, and other factors associated with the particular design. By performing the cost analysis and performance analysis in parallel, the compiler substantially reduces overall filter design cycle time as compared to conventional approaches to filter synthesis."

Consequently, it is respectfully submitted that a filter resource estimator is thoroughly described throughout the specification at both a high level and in detail sufficient to meet the written description requirement and to enable one of skill in the art to make and use the invention at the time the application was filed.

The Examiner rejected claims 1 and 16 under 35 U.S.C. 102(e) as being anticipated by Dick. Dick notes that "The equations that define the transfer function of predictor filter 40 ... should be implemented in a mathematical modeling environment, such as Matlab, and simulations [are] performed until a predictor length that satisfied the specific problem is

determined experimentally." (column 7, lines 23-30) Dick proceeds to noted that "in the present invention, the multipliers (4x12 bit) each consume only 8 CLBS. Therefore, even including the additional resources required to implement modulator 12, the CLB count is 3002. Thus, the present invention consumes only 39% of the logic resources of a prior art direct implementation." (column 7, lines 62-67).

Claims 1 and 16 explicitly recite a filter compiler comprising "a filter resource estimator coupled to the filter spectral response simulator for estimating an implementation cost of the filter." Dick does not teach or suggest a filter compiler including a "filter resource estimator" nor does it teach or suggest a "filter resource estimator coupled to the filter spectral response simulator." The Examiner argues that Dick describes a filter spectral response simulator (4:8-12). The material cited by the Examiner only notes that the FIR filter "can be configured to provide a variety of transfer functions, including low pass, high pass, and bandpass. As known by those skilled in the art, the desired transfer function is determined by selection of filter coefficients a.sub.0 and a.sub.N-1."

No "resource estimator is coupled to the filter spectral response simulator." The Examiner argues that Dick describes a filter resource estimator. However, the material cited by the Examiner only notes that "In a prior art implementation ... the total cost of a direct implementation of a FIR filter is 7672 CLBs... In contrast, in the present invention, ... the CLB count is 3002. Thus, the present invention consumes only 39% of the logic resources of a prior art direct implementation" (7:51-57). The material cited by the Examiner does not teach or suggest a filter resource estimator and mentions only a resource calculation. Dick makes no mention of having "filter resource estimator" "coupled to the filter spectral response simulator for estimating an implementation cost of the filter" as recited in the claims. Consequently, the rejection to independent claims 1 and 16 is believed overcome.

The Examiner argued that on page 8 of the 12/17/04 office action that "it is understood to one skilled in the art that after the filter is designed using the simulator, the estimate of the resources, or "real estate" the design will take up on the FPGA will be determined and once the design meets the requirements of the specification in terms of performance and resources, the design is then compiled for implemention on the FPGA."

However, neither Dick nor any understanding by one of skilled in the art teaches or suggests a "resource estimator is coupled to the filter spectral response simulator." The Examiner is believed to be referring to a prior art implementation described in the Background section of the present application. More specifically, "Based upon the desired filter response, the behavioral characteristics of the FIR filter are then determined based upon floating-point values that are converted to fixed-point filter coefficients. Once the particular filter coefficients have been calculated, the an interim hardware filter architecture is determined. By hardware filter architecture it is meant whether the FIR filter is to be configured as a parallel or serial type FIR filter. In some applications, a serial type FIR filter configuration may be appropriate whereas in other applications a parallel type FIR filter configuration may be appropriate. A simulation must then be iteratively run on the interim hardware filter architecture to ascertain whether or not FIR filter, as currently configured, meets the original design specifications. Once an appropriate filter design has been established based upon an acceptable simulation run, the FIR filter design is synthesized and fitted to a target PLD by an appropriate placing and routing program. Typical cycle times for the conventional FIR filter design cycle described above take on the average, at least 6 weeks to complete." (page 3, line 13 – page 4, line 6)

Synthesizing and fitting a design to a target PLD is not a "resource estimator is coupled to the filter spectral response simulator."

The Examiner rejected claim 37 under 35 U.S.C. 102(3) as being unpatentable over Dick and the Examiner rejected claim 41 under 35 U.S.C. 103(a) as being unpatentable over Dick in view of Samaraki. The Examiner argues that Dick (Column 8, Lines 11-14 and 38-41) teaches "applying a first clock rule when an input data width is less than or equal to an interpolation factor; and applying a second clock rule when an input data width is greater than the interpolation factor." The Applicants respectfully disagree. Neither Dick nor Samaraki even mention data widths. The material cited by the Examiner in Dick only describes sampling rates. Sampling rates are not data widths. Samaraki makes no mention of data widths. Consequently, the rejection to independent claims 37 and 41 are believed overcome.

In light of the above remarks relating to independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the

prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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